## REMARKS

The present application was filed on February 11, 2004 with claims 1 through 21. Claims 1-21 are presently pending in the above-identified patent application

In the Office Action, the Examiner rejected claims 11, 12, and 16-18 under 35 U.S.C. §102(b) as being anticipated by Leighton et al (United States Patent Number 6,512,646), and rejected claims 13, 14, and 19 under 35 U.S.C. §103(a) as being unpatentable over Leighton et al. The Examiner indicated that claims 1-10 are allowed, and that claims 15, 20, and 21 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Independent Claims 11 and 17

Independent claims 11 and 17 were rejected under 35 U.S.C. §102(b) as being anticipated by Leighton et al. Regarding claim 1, the Examiner asserts that Leighton discloses means for shunting ($Q_7$, $Q_8$) at least a portion of the current that would otherwise pass through the at least one resistor during an overshoot mode (col. 5, lines 7-42).

The present disclosure teaches that

> an ***impedance matched*** *write circuit* is provided that *shunts one or more* ***matching*** *resistors*. The impedance matched write circuit includes an interconnect for connecting to a write head and *at least one resistor between a control voltage and the interconnect* ***for impedance matching to the interconnect***. In one implementation, *a transistor is connected across the resistor to shunt current that would otherwise pass through the resistor during an overshoot mode*. The transistor may be a P-Channel Metal Oxide Silicon (PMOS) transistor or a combination of PMOS and NMOS transistors. A gate voltage of the transistor is controlled by a source such that the transistor is turned on in an overshoot mode and turned off during a steady state mode.
> (Page 2, lines 11-19; emphasis added.)

Applicants note that a "shunt" is defined as "a conductor having low resistance in ***parallel with another device*** to divert a fraction of the current." (See, dictionary.com.) A person of ordinary skill in the art would ***not*** view transistors $Q_7$, $Q_8$ as "shunting" resistors $R_{PA1}$ and $R_{PA2}$, respectively. Independent claims 11 and 17 require *means for* ***shunting*** *at least a portion of the current that would otherwise pass through said at least one resistor during an overshoot mode*

Thus, Leighton et al. do not disclose or suggest means for shunting at least a portion of the current that would otherwise pass through said at least one resistor during an overshoot mode, as required by independent claims 11 and 17.

Dependent Claims 2-10, 12-16 and 18-21

Dependent claims 12, 16, and 18 were rejected under 35 U.S.C. §102(b) as being anticipated by Leighton et al., and claims 13, 14, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Leighton et al.

Claims 2-10, 12-16, and 18-21 are dependent on claims 1, 11, and 17, respectively, and are therefore patentably distinguished over Leighton et al because of their dependency from independents claim 1, 11, and 17 for the reasons set forth above, as well as other elements these claims add in combination to their base claim. The Examiner has already indicated that claims 1-10 are allowed, and that claims 15, 20, and 21 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

All of the pending claims, i.e., claims 1-21, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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